

UNITED STATES DISTRICT COURT
EASTERN DISTRICT OF TEXAS
MARSHALL DIVISION

NETLIST, INC.

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD, et al.

Defendants.

Civil Action No. 2:22cv-00293-JRG
(Lead Case)

NETLIST, INC.

Plaintiff,

v.

MICRON TECHNOLOGY INC., et al.

Defendants.

Civil Action No. 2:22cv-00294-JRG

**JOINT NOTICE OF MOOTNESS REGARDING
CONSTRUCTION OF CLAIMS NO LONGER ASSERTED**

Defendants Samsung Electronics Co., Ltd. et al. (“Samsung”) and Micron Technology Texas, LLC et al. (“Micron”) and Plaintiff Netlist, Inc. (“Netlist”) respectfully submit this notice of mootness regarding the construction of certain claims of U.S. Patent No. 7,619,912 (“the ’912 patent”) which are no longer asserted in these actions.

After this Court’s Order on Samsung’s motion for summary judgment of intervening rights, Netlist withdrew its infringement allegations against Defendants’ DDR2 and DDR3 products. Specifically, Netlist has withdrawn its assertion of claims 1, 3, 4, 6, 8, 10, 11, 15, 18, 19, 20, 22, 24, 27, 28, 29, 31, 32, 34, 36, 37, 38, 39, 40, 41, 43, 45, 46, 47, 50, 52, 53, 54, 55, 56,

57, 58, 59, 60, 62, 63, 64, 65, 69, 70, 71, 72, 73, 74, 75, 77, and 80–91 of the '912 patent (“the Amended Claims”) in these actions. Netlist maintains its infringement allegations against Defendants’ DDR4 products.

Thus, the parties respectfully notify the Court that there is no longer a live dispute regarding the construction of the “wherein” clauses recited in the Amended Claims (i.e., the terms numbered 5, 6, 7, 8, 9, and 10 in the joint claim construction chart, *see* Dkt. No. 160-1 at 2-6, reproduced below).

- “wherein the logic element generates gated column access strobe (CAS) signals or chip-select signals of the output [control] signals in response at least in part to (i) the [at least one] row address signal, (ii) the bank address signals, and (iii) the [at least one] chip-select signal of the [set/plurality] of input [control] signals and (iv) the PLL clock signal” (Claims 1, 15, 28, 39);
- “wherein the logic element responds to at least (i) a row address bit of the at least one row/column address signal, (ii) the bank signals, and (iii) the at least one chip-select signal of the set of input control signals and (iv) the PLL clock by generating a first number of chip-select signals of the set of output control signals, the first number of chip-select signals generated by the logic element equal to the first number of ranks, and the at least one chip-select signal of the set of input control signals comprises a second number of chip-select signals equal to the second number of ranks” (Claim 77);
- “wherein the generation of the first number of chip-select signals of the output control signals by the logic element is based on the logic element responsive at least in part to (i) the at least one row address signal, (ii) the bank address signals, and (iii) the at least one chip-select signal of the set of input control signals received by the logic element and (iv) the clock signals received from the phase-lock loop device” (Claim 80);
- “wherein the logic element responds to at least the at least one row address signal, the bank address signals, and the at least one chip-select signal of the set of input [control] signals and the PLL clock signal by generating a number of rank-selecting signals of the set of output [control] signals that is greater than double or equal to double the number of chip-select signals of the set of input [control] signals” (Claim 82, 86);
- “wherein the logic element responds to at least (i) the row address signal, (ii) the bank address signals, (iii) and the one chip-select signal of the set of input control signals and (iv) the PLL clock signal by generating a number of rank-selecting signals of the set of output signals that is greater than double or equal to double the number of chip-select signals of the set of input control signals” (Claim 88);

- “wherein the logic element responds to at least (i) the at least one row signal, (ii) the bank address signals, (iii) and the second number of chip-select signals of the plurality of input signals and (iv) the PLL clock signal by generating the first number of chip-select signals of the plurality of output signals that is greater than double or equal to double the second number of chip-select signals of the plurality of input signals” (Claim 90).

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Respectfully submitted,

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CERTIFICATE OF SERVICE

I hereby certify that a true and correct copy of the foregoing document was filed electronically in compliance with Local Rule CV-5 on November 6, 2023. As of this date, all counsel of record have consented to electronic service and are being served with a copy of this document through the Court's CM/ECF system under Local Rule CV-5(a)(3)(A).

/s/ Francis J. Albert